WHAT IS CLAIMED IS:

1. A magnetic memory, comprising:

at least two magnetic memory cells configured to store data; and

a control system configured to at least twice obtain parametric values from the magnetic memory cells and generate a corresponding compressed fault map using the parametric values, wherein at least one of the compressed fault maps is compared to a previous one of the compressed fault maps and an indication is provided if there are differences.

2. The magnetic memory of claim 1, wherein each one of the compressed fault maps includes at least one error detection code result which is calculated over the addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, and wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range.

3. The magnetic memory of claim 2, wherein each one of the compressed fault maps includes at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

4. The magnetic memory of claim 1, wherein each one of the compressed fault maps includes at least one error detection code result which is calculated over fault types and corresponding addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range, and wherein the corresponding one of the

parametric values is compared to the expected range to infer a corresponding one of the fault types.

5. The magnetic memory of claim 4, wherein each one of the compressed fault maps includes at least two error detection code results, wherein each one of the error detection code results is calculated over one of the fault types and the corresponding addresses of all of the magnetic memory cells which have a same one of the fault types.

6. The magnetic memory of claim 4, wherein each one of the compressed fault maps includes at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the fault types and the corresponding addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

7. The magnetic memory of claim 4, wherein the fault types and the corresponding addresses of the magnetic memory cells are sorted into a numerical order before the error detection code result is calculated.

8. The magnetic memory of claim 4, wherein the error detection code result is calculated using a cyclic redundancy check code.

9. The magnetic memory of claim 1, wherein the one of the compressed fault maps is compared to the previous one of the compressed fault maps by comparing bits of the one of the compressed fault maps to bits of the previous one of the compressed fault maps, wherein an indication is provided if there are differences.

10. The magnetic memory of claim 1, wherein the previous one of the compressed fault maps is generated using parametric values obtained from the

magnetic memory cells the first time that the control system obtains the parametric values from the magnetic memory cells.

11. The magnetic memory of claim 1, wherein the previous compressed fault map is stored in at least one of the magnetic memory cells.

12. A controller for a magnetic memory which includes at least one array of magnetic memory cells configured to store data, comprising:

firmware configured to store a procedure for obtaining parametric values from magnetic memory cells in the array of magnetic memory cells and generating a compressed fault map using the parametric values; and

a microcontroller configured to execute the procedure a first time to generate a first compressed fault map, wherein the microcontroller executes the procedure at one or more time intervals after the first time and compares a second compressed fault map generated at each time interval to the first compressed fault map and provides an indication if there are differences between the second compressed fault map and the first compressed fault map.

13. The controller of claim 12, wherein the first compressed fault map and the second compressed fault map each include at least one error detection code result which is calculated over the addresses of the magnetic memory cells in the array which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, and wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range.

14. The controller of claim 13, wherein the first compressed fault map and the second compressed fault map each include at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the addresses of the magnetic memory cells which have the fault and are within a same one of the

address ranges, wherein each one of the addresses is within only one of the address ranges.

15. The controller of claim 12, wherein the first compressed fault map and the second compressed fault map each include at least one error detection code result which is calculated over fault types and corresponding addresses of the magnetic memory cells in the array which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range, and wherein the corresponding one of the parametric values is compared to the expected range to infer a corresponding one of the fault types.

16. The controller of claim 15, wherein the first compressed fault map and the second compressed fault map each include at least two error detection code results, wherein each one of the error detection code results is calculated over one of the fault types and the corresponding addresses of all of the magnetic memory cells in the array which have a same one of the fault types.

17. The controller of claim 15, wherein the first compressed fault map and the second compressed fault map each include at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the fault types and the corresponding addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

18. The controller of claim 17, wherein the microcontroller transfers, when the indication is provided, the data from the magnetic memory cells in at least one of the address ranges where at least one of the magnetic memory cells has the fault, to the magnetic memory cells in at least one of the address ranges where none of the magnetic memory cells have the fault.

19. A storage system, comprising:

at least two magnetic memory storage devices, each including at least one array of magnetic memory cells configured to store data; and

a control system configured to periodically obtain parametric values from magnetic memory cells in the magnetic memory storage devices and generate, using the parametric values, at least one error detection code result which is compared to a previous at least one error detection code result, wherein an indication is provided if there are differences.

20. The storage system of claim 19, wherein the error detection code result is calculated over the addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, and wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range, and wherein the control system transfers, when the indication is provided, the data from at least one of the magnetic memory storage devices wherein at least one of the magnetic memory cells has fault, to at least one of the magnetic memory storage devices where none of the magnetic memory cells have the fault.

21. The storage system of claim 20, wherein the error detection code result includes at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges, and wherein the control system transfers, when the indication is provided, the data from at least one of the address ranges wherein at least one of the magnetic memory cells has fault, to at least one of the address ranges where none of the magnetic memory cells have the fault.

22. The storage system of claim 19, wherein the error detection code result is calculated over fault types and corresponding addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range, wherein the corresponding one of the parametric values is compared to the expected range to infer a corresponding one of the fault types, and wherein the control system transfers, when the indication is provided, the data from at least one of the magnetic memory storage devices wherein at least one of the magnetic memory cells has fault, to at least one of the magnetic memory storage devices where none of the magnetic memory cells have the fault.

23. The storage system of claim 22, wherein the error detection code result includes at least two error detection code results, wherein each one of the error detection code results is calculated over one of the fault types and the corresponding addresses of all of the magnetic memory cells which have a same one of the fault types, and wherein the control system transfers, when the indication is provided, the data from at least one of the magnetic memory storage devices wherein at least one of the magnetic memory cells has the fault, to at least one of the magnetic memory storage devices where none of the magnetic memory cells have the fault.

24. The storage system of claim 22, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the fault types and the corresponding addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges, and wherein the control system transfers, when the indication is provided, the data from at least one of the address ranges wherein at least one of the magnetic memory cells has fault, to at least one of the address ranges where none of the magnetic memory cells have the fault.

25. A magnetic memory, comprising:

at least two magnetic memory cells configured to store data; and

control means configured to periodically obtain parametric values from the magnetic memory cells and generate a corresponding compressed fault map using the parametric values, wherein at least one of the compressed fault maps is compared to a previous one of the compressed fault maps and an indication is provided if there are differences.

26. The magnetic memory of claim 25, wherein the control means includes:

first means configured to store a procedure for obtaining parametric values from the magnetic memory cells and generating the corresponding compressed fault map using the parametric values; and

second means configured to periodically execute the procedure and generate the corresponding compressed fault map, wherein the second means compares the compressed fault map to a previous one of the compressed fault maps and provides the indication if there are differences.

27. A method of detecting degradation in at least two magnetic memory cells, comprising:

periodically obtaining parametric values from the magnetic memory cells;

generating a compressed fault map each time the parametric values are obtained;

comparing at least one of the compressed fault maps to a previous one of the compressed fault maps; and

providing an indication if there are differences.

28. The method of claim 27, wherein generating a compressed fault map comprises calculating at least one error detection code result over the addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, and

wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range.

29. The method of claim 28, wherein generating a compressed fault map comprises calculating each one of at least two error detection code results, for a corresponding one of at least two address ranges, over the addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

30. The method of claim 27, wherein generating a compressed fault map comprises calculating at least one error detection code result over fault types and corresponding addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range, and wherein the corresponding one of the parametric values is compared to the expected range to infer a corresponding one of the fault types.

31. The method of claim 30, wherein generating a compressed fault map comprises calculating each one of at least two error detection code results over one of the fault types and the corresponding addresses of all of the magnetic memory cells which have a same one of the fault types.

32. The method of claim 30, wherein generating a compressed fault map comprises calculating each one of at least two error detection code results, for a corresponding one of at least two address ranges, over the fault types and the corresponding addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

33. The method of claim 32, wherein providing an indication further comprises transferring the data from the magnetic memory cells in at least one of the address ranges where at least one of the magnetic memory cells has the fault, to the magnetic memory cells in at least one of the address ranges where none of the magnetic memory cells have the fault.

34. A method of detecting degradation in a magnetic memory which includes at least one array of magnetic memory cells configured to store data, comprising:

executing a procedure for obtaining parametric values from magnetic memory cells in the array of magnetic memory cells;

generating a first compressed fault map from the parametric values;

for each one of at least one time intervals:

executing the procedure to generate a second compressed fault map;

comparing the second compressed fault map to the first compressed fault map; and

providing an indication if there are differences between the second compressed fault map and the first compressed fault map.

35. The method of claim 34, wherein generating the first compressed fault map or generating a second compressed fault map includes sorting the fault types and the corresponding addresses of the magnetic memory cells into a numerical order before the first compressed fault map or the second compressed fault map is generated.